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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,728	09/26/2003	Hironobu Kariyazono	59520 (48229)	9422

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EXAMINER
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ROSE, KIESHA L

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/672,728

**Applicant(s)**

KARIYAZONO, HIRONOBU

**Examiner**

Kiesha L. Rose

**Art Unit**

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) 1-12,20-23,25-28,32 and 33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-19,24 and 29-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

This Office Action is in response to the election filed 21 December 2004.

### ***Election/Restrictions***

Claims 1-12,20-23,25-28 and 32-33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of making a semiconductor device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 21 December 2004.

Applicant's election without traverse of claims 13-19,24 and 29-31 in the reply filed on 21 December 2004 is acknowledged.

### ***Specification***

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

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The abstract of the disclosure is objected to because it should be directed to the product of the invention and not geared toward the method of making the invention.

Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 13-16,18-19,24 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. Patent 6,483,152).

Kim discloses a semiconductor device (Figs. 1c-d) that contains a silicon semiconductor layer (1), a MOS transistor formed on the semiconductor layer, a resistive layer (41) formed on semiconductor layer through an insulating layer (2), the MOS transistor comprises a silicon oxide gate insulating layer (3) and a gate electrode (42) formed on gate insulating layer, where the gate electrode comprises a multi-layered structure including a polysilicon layer (42) and a metal layer (14) formed on tungsten, where the resistive layer is formed of polysilicon and a protective layer (12) formed on the resistive layer to cover the resistive layer.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 17 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Kanda et al. (U.S. Publication 2003/0034531).

Kim discloses all the limitations except for a high and low breakdown voltage transistor. Whereas Kanda discloses a semiconductor device (Fig. 28) that contains a MOS high voltage breakdown transistor (HV) and a low voltage breakdown transistor (LV) of insulated gate types formed on a semiconductor layer (100), where the high voltage transistor includes a proof voltage between a source and drain, which is different from the low breakdown voltage transistor. The high and low breakdown voltage transistors are formed so the high voltage act as an actuation output module to have a high withstanding breakdown voltage and the low voltage transistor to act as a logic module for controlling the actuation output module. (Page 1, Paragraph 4)

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate high and low breakdown voltage transistors so the high voltage act as an actuation output module to have a high withstanding breakdown voltage and the low voltage transistor to act as a logic module for controlling the actuation output module as taught by Kanda.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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